

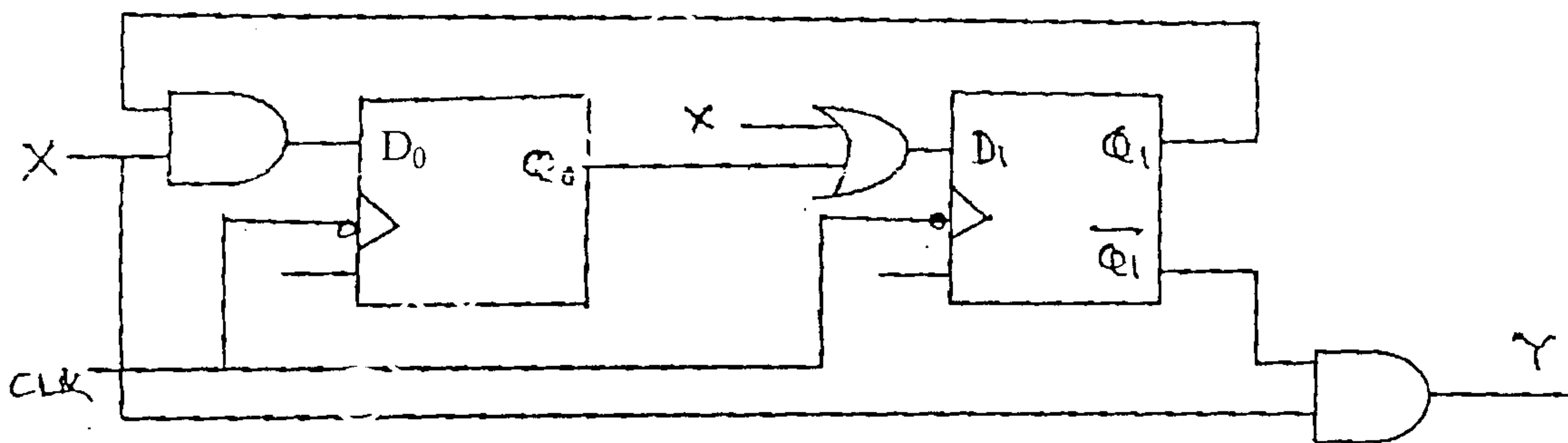
QP Code :4818

(3 Hours)

[ Total Marks : 80

- N.B.: (1) Question No.1 is compulsory.  
 (2) Solve any three from remaining five questions.  
 (3) Draw neat diagram wherever necessary.

1. (a) Explain the current sinking and sourcing when two standard TTL gates are connected. 5
- (b) Explain glitch problem of ripple counter along with waveform. 5
- (c) Draw truth table and circuit of JK flip flop using NAND gates. 5
- (d) Draw internal block diagram of IC 7490. 5
2. (a) Design 4 bit ring counter using IC 74194 and draw its output waveform. 10
- (b) Discuss CPLD XC 9500 architecture with neat block diagram. Describe main features. 10
3. (a) Design MOD 11 synchronous counter using T flip flop. 10
- (b) Identify the circuit shown in figure. Write the state table and draw state diagram for the same. 10



4. (a) Implement 10 bit comparator using IC 7485. 10
  - (b) Simplify following logic function and realize using NOR gates. 10
- $$f(w,x,y,z) = \pi M(1, 2, 3, 7, 10, 11) + d(0, 15)$$
- $$f(w,x,y,z) = \pi M(3, 4, 5, 6, 7, 10, 11, 15)$$

5. (a) Identify indistinguishable state in following state table and obtain minimized state diagram 10

PS	X = 0		X = 1	
	NS	Output	NS	Output
A	A	0	A	0
B	A	1	F	1
C	D	0	E	0
D	A	1	G	0
E	B	0	C	0
F	D	0	D	0
G	B	0	C	0

(b) Draw a circuit diagram of a CMOS inverter. Draw its transfer Characteristics and explain its operation. 10

6. Write a short note on (any three) ??

- (i) K-map.
- (ii) Automatic Test Pattern Generation (ATPG).
- (iii) Mealy and Moore sequential machine.
- (iv) SR flip flop.